REMARKS

Claims 5-8 and 10-12 are pending. Claim 9 is canceled and claims 5, 7, 8 and 10 are amended.

CLAIM OBJECTIONS

Claims 7-8 have been objected to due to minor informalities. As per the Examiner's comments, claims 7 and 8 have been amended to recite the method of claim 5 rather than the semiconductor device in claim 5.

CLAIM REJECTION - U.S.C. § 102

Claims 5-7 and 9-12 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Hirabayashi (U.S. Patent No. 5,614,445). Applicant respectfully traverses this rejection.

Hirabayashi discloses a method of manufacturing a semiconductor wafer. As shown in Figs. 6-8, this silicon wafer includes scribe lines which are formed of window openings 6' and corresponding dummy etched grooves 6. The dummy etched grooves 6 found in the position of the window openings 6' plasma etching the substrate. The grooves 6 are then implanted with boron ions and a sidewall insulating film 8 is formed in the grooves 6. Then, the grooves 6 are completely filled with polycrystalline silicon 9.

As a result, the scribe lines are formed of multiple materials in addition to the substrate. Therefore, Hirabayashi fails to disclose, "said scribe lanes ... containing only the semiconductor substrate," as recited in part by claim 5 as amended.

Hirabayashi also discloses n-wells 28 formed in the p-type substrate 22. As shown in Fig. 12, the n-wells 28 further contain two wells 29a and 30a of the same conductivity type. Therefore, Hirabayashi also does not disclose "a first conductive well area and a second conductive well area are separately formed within the deep well area, the first conductive well area is formed of the first conductivity type, and the second conductive well area is formed of the second conductivity type," as recited in part by claim 10.

Accordingly, claims 5 and 10 are allowable over the prior art. Regarding claims 6-8 and 11-12, these claims are allowable for at least the same reasons as their corresponding independent claims. Therefore, Applicant respectfully requests removal of this rejection.

Claims 5 and 8 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Kim et al. (U.S. Patent No. 6,159,826). Applicant respectfully traverses this rejection.

Kim et al. disclose a method of fabricating a semiconductor device. As shown in Figs. 3 and 4 of Kim et al., a plurality of semiconductor chip portions 32 are formed on a wafer 30. The chip portions 32 are separated by scribe lanes 34. As shown in Fig. 5, the scribe lanes 34 include an n-substrate, p-well, insulating layers and conductive patterns.

Due to the various features contained in the scribe lanes 34, one difference between Kim et al. and the claimed invention is that the scribe lanes of Kim et al. do not contain "only the semiconductor substrate," as recited in part by claim 5 as amended.

Accordingly, claim 5 is allowable over the prior art. Regarding claim 8, this claim is allowable for at least the same reasons as its corresponding independent claim 5. Therefore, Applicant respectfully requests removal of this rejection.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the rejection and allowance of claims 5-8 and 10-12 is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By James T. Eller, Jr. #39,538
Joseph A. Kolasch, #22,463

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

JAK/JES/mua:sld
0465-0751P

Attachment: Version with Markings to Show Changes Made

(Rev. 11/28/01)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claim 9 has been canceled.

The claims have been amended as follows:

5. (Amended) A method for manufacturing a semiconductor device comprising:

preparing a semiconductor substrate of a first conductivity type;

forming scribe lanes in the semiconductor substrate, said scribe lanes defining chip formation areas and containing only the semiconductor substrate;

forming a deep well area in each chip formation area, each deep well area having a second conductivity type opposite the first conductivity type; and

forming at least one well area within the deep well area.

7. (Twice Amended) The [semiconductor device] method of claim 5, wherein,

the first conductivity type is a p-type conductor; and

the second conductivity type is a n-type conductor.

8. (Twice Amended) The [semiconductor device] method of claim 5, wherein,

the first conductivity type is a n-type conductor; and

the second conductivity type is a p-type conductor.

10. (Twice Amended) [The method of claim 9, wherein] A method for manufacturing a semiconductor device comprising:

preparing a semiconductor substrate of a first conductivity type;

forming scribe lanes in the semiconductor substrate, said scribe lanes defining chip formation areas;

forming a deep well area in each chip formation area, each deep well area having a second conductivity type opposite the first conductivity type; and

wherein a first conductive well area and a second conductive well area are separately formed within the deep well area,

the first conductive well area is formed of the first conductivity type[;], and

the second conductive well area is formed of the second conductivity type.